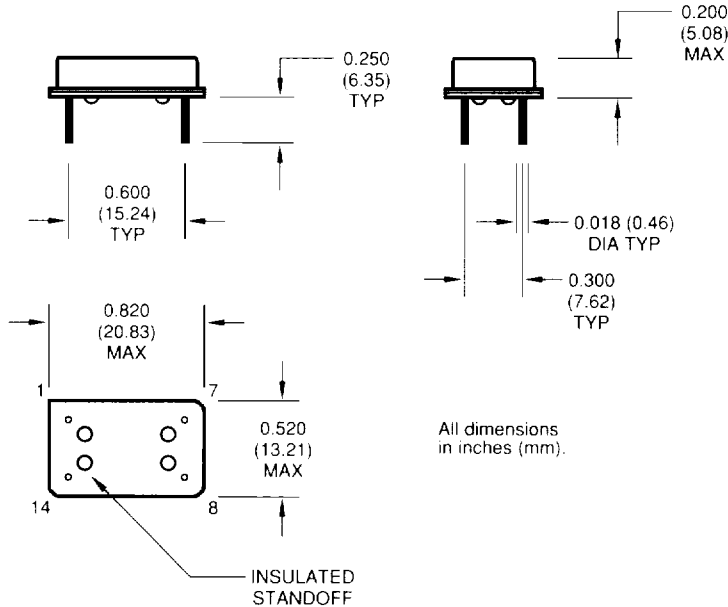


# MHO+ Series HCMOS Oscillators

## High Performance HCMOS/TTL Compatible Oscillators



<b>Part Marking and Numbering</b>	MHO+	1	3	F	A	D
<b>Product Series</b>	MHO+					
<b>Temperature Range</b>	1: 0°C to +70°C    2: -40°C to +85°C 3: -55°C to +105°C    4: -55°C to +125°C 5: -10°C to +85°C    6: -20°C to +70°C 7: 0°C to +85°C					
<b>Stability</b>	1: ± 1000 ppm    2: ± 500 ppm 3: ± 100 ppm    4: ± 50 ppm 5: ± 35 ppm    6: ± 25 ppm 7: +0/-200 ppm					
<b>Output Type</b>	F: Fixed    E: Enable/Disable (300.000 kHz and above) T: Tristate (1.000 to 67.000 MHz)					
<b>Symmetry/Logic Compatibility</b>	A: 40/60 CMOS/TTL    B: 45/55 TTL    C: 45/55 CMOS D: 45/55 both*    F: 40/60 TTL    G: 40/60 CMOS					
<b>Package/Lead Configurations</b>	D: DIP; Nickel Header    G: Gull Wing; Nickel Header					

\*Standard for frequencies less than 3.000 MHz

## Pin Connections

PIN	FUNCTION
1	N/C, Enable/Disable or Tristate
7	Circuit/Case Ground
8	Output
14	+ V <sub>dd</sub>

### ENABLE/DISABLE

Pin 1 high or floating: clock signal output  
Pin 1 low: output disables to logic "1"

### TRISTATE

Pin 1 high or floating: clock signal output  
Pin 1 low: output disables to high impedance

## Available Stabilities vs Temperature

T	S	1	2	3	4	5	6	7
1	A	A	S	A	A	A	A	A
2	A	A	A	A	A	A	A	A
3	P	P	P	P	N	N	N	P
4	P	P	P	N	N	N	N	P
5	A	A	A	A	A	A	A	A
6	A	A	A	A	A	A	A	A
7	A	A	A	A	A	A	A	A

Consult factory regarding availability of T-S combinations marked "P."

A = AVAILABLE    S = STANDARD  
P = PLANNED    N = NOT AVAILABLE

## Electrical Specifications

(Standard Operating Conditions 0°C to 70°C; V<sub>dd</sub> = 5.0 ±10% V DC)

PARAMETERS	Symmetry Types				A, B, C, D		F		G		UNITS
	TTL Load		CMOS Load		TTL Load		CMOS Load				
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
<b>Frequency Range</b>	.732 k	67.0 M	.732 k	67.0 M	50.1 M	80.0 M	50.1 M	80.0 M			kHz/ MHz
<b>Output Load</b>											
0.732 kHz to 2.990 MHz			5 TTL <sup>1</sup>								TTL/pF
3.000 to 67.000 MHz			10 TTL <sup>1</sup>								TTL/pF
50.010 to 80.000 MHz					10 TTL <sup>1</sup>				50 pF <sup>2</sup>		TTL/pF
<b>Symmetry*</b>											
0.732 kHz to 67.000 MHz	According to Symmetry code.										
50.010 to 80.000 MHz					40/60    60/40		60/40		40/60		%
<b>Logic "0" Level</b>			0.5		10% V <sub>dd</sub>		0.5		10% V <sub>dd</sub>		V
<b>Logic "1" Level</b>	(V <sub>dd</sub> -0.5)		90% V <sub>dd</sub>		(V <sub>dd</sub> -0.5)		90% V <sub>dd</sub>				V
<b>Rise/Fall Time**</b>											
0.732 kHz to 2.990 MHz			10		20.0						ns
3.000 to 67.000 MHz			5.0		10.0						ns
50.010 to 80.000 MHz							5.0		10.0		ns
<b>Supply Current</b>											
0.732 kHz to 2.990 MHz			15.0		15.0						mA
3.000 to 25.990 MHz			25.0		25.0						mA
26.000 to 67.000 MHz			55.0		60.0						mA
50.010 to 80.000 MHz							55.0		60.0		mA

1- See load circuit #1 on page 32; 2- See load circuit #2 on page 32.

\*Symmetry is measured at 1.4 V with TTL load, and at V<sub>dd</sub>/2 with HCMOS load.

\*\*Rise/fall times are measured between 0.5V and 2.4V with TTL load, and between 10% V<sub>dd</sub> and 90% V<sub>dd</sub> with HCMOS load.

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